which form gate zones of these transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$; $0<x<1$) situated between said polycrystalline silicon layer and the gate oxide, along with an amorphous silicon layer which is formed, characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium.

REMARKS

This application has been carefully reviewed in light of the Office Action dated March 19, 2003. Claims 1-4 remain pending in this application. Claim 1 is the independent claim. Favorable reconsideration is respectfully requested.

The Office Action rejected Claims 1-2 and 4 under 35 U.S.C. § 102(b) as being anticipated by Hwang et al. (EU Patent 0614226; hereinafter "Hwang"). In addition, the Office Action also rejected Claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Hwang in view of both Hwang and Song (U.S. Patent No. 5,760,420). Applicant respectfully submits that the pending application and claims are patentable for at least the following reasons.

Applicant's Claim 1 recites: "A semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate and